Experiment No. 2: BJT and FET Biasing for Stable Operation

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1. Aim of the Experiment

To design and implement different biasing schemes for Bipolar Junction Transistor (BJT) and Field-Effect Transistor (FET) amplifiers, and to analyze their Quiescent point (Q-point) stability under varying conditions.

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2. Objectives

Upon successful completion of this experiment, students will be able to:

- Understand the fundamental concept and necessity of transistor biasing.
- Design and construct a BJT Voltage Divider Bias circuit to achieve a specified Q-point.
- Analyze the theoretical and practical Q-point of a BJT Voltage Divider Bias circuit.
- Design and construct a BJT Fixed Bias circuit.
- Compare and contrast the stability of BJT Fixed Bias and Voltage Divider Bias circuits through practical observation of Q-point variations.
- Design and construct an N-channel JFET Self-Bias circuit.
- Analyze the theoretical and practical Q-point of a JFET Self-Bias circuit.
- Critically discuss the advantages and disadvantages of each biasing scheme in terms of stability, component count, and suitability for various applications.

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3. Apparatus and Components Required

S. No.	Item	Specification / Type	Quantity
1.	DC Regulated Power Supply	0-30V, 1A (or similar)	1
2.	Digital Multimeter (DMM)	For voltage, current, and resistance measurements	1
3.	Breadboard	Standard size	1
4.	NPN BJT	BC547 (or 2N3904, 2N2222, etc.)	2-3
5.	N-channel JFET	J201 (or 2N5457, 2N3819, etc.)	1

6.	Resistors	Various standard E12/E24 series (e.g., 100Ω, 220Ω, 470Ω, 1kΩ, 2.2kΩ, 4.7kΩ, 10kΩ, 22kΩ, 47kΩ, 100kΩ, 470kΩ, 560kΩ, 1MΩ)	As per design
7.	Potentiometer (Optional)	10kΩ (for fine-tuning, if desired)	1
8.	Connecting Wires	Assorted	As needed

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4. Theoretical Background

4.1. Introduction to Transistor Biasing

Transistors (BJTs and FETs) are active devices primarily used for amplification and switching. For a transistor to function correctly as an amplifier, it must be set up to operate in its "active region" (for BJTs) or "saturation/pinch-off region" (for JFETs) when no input signal is applied. This process of establishing the appropriate DC voltages and currents in a transistor circuit is called **biasing**. The specific DC operating point defined by these voltages and currents is known as the **Quiescent Point (Q-point)**.

The Q-point is critical because:

- It determines the range of AC signal swing that the amplifier can handle without distortion (clipping). An ideal Q-point is typically located near the center of the DC load line to allow for maximum symmetrical output swing.
- It directly affects the gain and linearity of the amplifier.

4.2. Importance of Q-point Stability

Transistor parameters are not perfectly constant. They can vary significantly due to:

- **Manufacturing Tolerances:** Even transistors of the same part number can have different parameter values (β for BJTs, IDSS and VP for JFETs).
- **Temperature Variations:** Transistor characteristics are highly temperature-dependent. For instance, β of a BJT generally increases with temperature, and leakage currents also increase.
- **Aging:** Over time, component characteristics can drift.

If a biasing circuit is not designed to be stable, these variations will cause the Q-point to shift. A shifted Q-point can lead to:

- **Distortion:** The amplifier might clip the signal prematurely if the Q-point moves too close to the cutoff or saturation region.

- **Reduced Gain:** The amplifier might operate in a non-optimal region, leading to lower than expected amplification.
- **Malfunction:** In extreme cases, the transistor might switch fully ON (saturation) or fully OFF (cutoff), failing to amplify at all.

Therefore, a primary goal of biasing circuit design is to ensure a stable Q-point, meaning it remains relatively constant despite unavoidable variations in transistor parameters and environmental conditions.

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5. BJT Biasing Schemes

We will focus on two common BJT biasing methods: Fixed Bias and Voltage Divider Bias.

5.1. BJT Fixed Bias (Base Bias)

5.1.1. Circuit Diagram:

[Conceptual Diagram of NPN BJT Fixed Bias]

- **VCC** (Collector Supply Voltage) connects to the collector via **RC** (Collector Resistor).
- **VCC** connects to the base via **RB** (Base Resistor).
- Emitter is directly connected to Ground.

5.1.2. Principle of Operation: The base resistor RB limits the base current IB from VCC. This sets up a base current, which in turn establishes the collector current IC=βDCIB. The collector-emitter voltage VCE is then determined by the voltage drop across RC.

5.1.3. Formulas:

1. **Base Current (IB):** The voltage across RB is VCC−VBE. IB=RBVCC−VBE (For silicon BJTs, VBE≈0.7V)
2. **Collector Current (IC):** IC=βDCIB (βDC is the DC current gain, typically obtained from the transistor datasheet).
3. **Collector-Emitter Voltage (VCE):** VC=VCC−ICRC Since the emitter is at ground, VE=0V. Therefore, VCE=VC−VE=VCC−ICRC

5.1.4. Disadvantages and Stability Issues: The major drawback of fixed bias is its **extreme sensitivity to βDC variations**. From the formulas, IC is directly proportional to βDC. If βDC doubles (which can happen due to temperature increase or simply using a different transistor of the same type), IC also doubles. This drastic shift in IC directly moves the Q-point, often pushing it into saturation or cutoff, leading to severe signal distortion. Therefore, fixed bias is rarely used in practical amplifier designs where stability is crucial.

5.2. BJT Voltage Divider Bias (Self-Bias / Emitter Bias for BJT)

5.2.1. Circuit Diagram:

[Conceptual Diagram of NPN BJT Voltage Divider Bias]

- **VCC** connects to the collector via **RC** and to the base via **R1**.
- The base is connected to ground via **R2**, forming a voltage divider with R1.
- The emitter is connected to ground via **RE** (Emitter Resistor).

5.2.2. Principle of Operation: This biasing method is the most popular due to its excellent stability. Resistors R1 and R2 form a voltage divider that sets a stable voltage at the base (VB). The emitter resistor RE provides crucial negative feedback for stability. If IC (and thus IE) tries to increase (e.g., due to temperature rise), the voltage drop across RE (VE=IERE) increases. Since VB is relatively fixed, an increase in VE causes VBE=VB−VE to decrease. A decrease in VBE reduces the base current IB, which in turn counteracts the initial increase in IC, effectively stabilizing the Q-point.

5.2.3. Formulas (Exact and Approximate):

There are two main approaches for analysis:

a) Exact Analysis (Thevenin's Equivalent Circuit at Base):

- **Thevenin Voltage (VTH):** This is the open-circuit voltage at the base. VTH=VCC×R1+R2R2
- **Thevenin Resistance (RTH):** This is the equivalent resistance looking back from the base, with VCC shorted to ground. RTH=R1∣∣R2=R1+R2R1R2
- Now, consider the base-emitter loop: VTH=IBRTH+VBE+IERE. Substitute IE=(βDC+1)IB: VTH=IBRTH+VBE+(βDC+1)IBRE VTH−VBE=IB[RTH+(βDC+1)RE]
- **Base Current (IB):** IB=RTH+(βDC+1)REVTH−VBE
- **Collector Current (IC):** IC=βDCIB
- **Emitter Current (IE):** IE=IB+IC=(βDC+1)IB≈IC (since βDC>>1)
- **Collector-Emitter Voltage (VCE):** VC=VCC−ICRC VE=IERE≈ICRE VCE=VC−VE=VCC−ICRC−IERE≈VCC−IC(RC+RE)

b) Approximate Analysis (Simplified Approach): This method is valid when the current through the voltage divider (IR2) is much larger than the base current (IB). A common rule of thumb is IR2≥10IB. This ensures that the base voltage VB is primarily determined by R1 and R2, and is relatively independent of βDC.

- **Base Voltage (VB):** VB≈VCC×R1+R2R2
- **Emitter Voltage (VE):** VE=VB−VBE
- **Emitter Current (IE):** IE=REVE
- **Collector Current (IC):** IC≈IE
- **Collector-Emitter Voltage (VCE):** VCE=VCC−IC(RC+RE)

5.2.4. Design Procedure for Voltage Divider Bias: The goal is to choose resistor values (R1,R2,RC,RE) to achieve a desired Q-point (IC,VCE).

1. **Choose Target IC and VCE:** Select your desired Q-point. A good starting point for VCE is VCC/2 for maximum symmetrical swing. For IC, a typical value for small-signal amplifiers is 1mA to 10mA.
2. **Determine VE and Calculate RE:** To ensure stability and provide sufficient voltage swing, set VE typically between 10% and 20% of VCC. A common choice is

VE≈0.15VCC. RE=IEVE≈ICVE (Use a standard resistor value close to the calculated value).

3. **Determine VC and Calculate RC:** VC=VCE+VE. RC=ICVCC−VC (Use a standard resistor value). *Self-check:* RC+RE should be less than VCC/IC to keep the transistor out of saturation.
4. **Determine VB:** VB=VE+VBE (using VBE≈0.7V for silicon BJT).
5. **Calculate R1 and R2:** To ensure stability (i.e., making VB less dependent on β), the current flowing through R2 (IR2) should be at least 10 times the base current (IB). IB=βminIC (Use the minimum β value from the datasheet to ensure worst-case stability). Choose IR2=10×IB. Now, use the voltage divider formulas: R2=IR2VB R1=IR2+IBVCC−VB (Use standard resistor values for R1 and R2). *After selecting standard values for R1,R2,RC,RE, it's good practice to recalculate the actual Q-point using the Exact Analysis method to confirm it's close to the desired point.*

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6. JFET Biasing Scheme

We will focus on the Self-Bias scheme for JFETs.

6.1. JFET Self-Bias

6.1.1. Circuit Diagram:

[Conceptual Diagram of N-channel JFET Self-Bias]

- **VDD** (Drain Supply Voltage) connects to the drain via **RD** (Drain Resistor).
- The gate is connected to ground via a very large resistor **RG** (typically 1MΩ or more) to provide a DC path for the gate and ensure VG=0V. This resistor does not significantly affect the DC biasing because the gate current of a JFET is practically zero.
- The source is connected to ground via **RS** (Source Resistor).

6.1.2. Principle of Operation: The self-bias configuration is widely used for JFETs. The drain current ID flows through the source resistor RS, creating a voltage drop VS=IDRS. Since the gate is at ground (VG=0V), the gate-source voltage is VGS=VG−VS=0−IDRS=−IDRS. This means VGS is inherently negative (for N-channel JFETs), which is exactly what's required to operate the JFET in its active (pinch-off) region. This negative feedback (increase in ID makes VGS more negative, which tends to reduce ID) provides good Q-point stability.

6.1.3. Key Formulas (Shockley's Equation): The relationship between ID and VGS for a JFET is described by Shockley's Equation: ID=IDSS(1−VPVGS)2 where:

- ID is the Drain Current.
- IDSS is the Drain-Source Saturation Current (the maximum drain current when VGS=0V).
- VGS is the Gate-Source Voltage.

- VP is the Pinch-off Voltage (also denoted as VGS(off), the value of VGS at which ID ideally becomes zero). Note that VP is a negative value for N-channel JFETs.

Also, for the self-bias circuit: VGS=−IDRS

6.1.4. Design Procedure for JFET Self-Bias (Analytical/Graphical):

1. **Obtain JFET Parameters:** Identify IDSS and VP from the JFET datasheet. Be aware that these values can vary significantly even for the same part number.
2. **Choose Target ID:** Select a desired drain current (ID) for your Q-point. A common choice is to set ID≈IDSS/2 for good linearity and headroom.
3. **Calculate VGS:** Substitute the target ID, IDSS, and VP into Shockley's Equation and solve for VGS: IDSSID=(1−VPVGS)2 IDSSID  =1−VPVGS
VPVGS=1−IDSSID  VGS=VP(1−IDSSID )
4. **Calculate RS:** Using the calculated VGS and target ID: RS=−IDVGS (Since VGS will be negative for N-channel JFETs, RS will be positive). (Use a standard resistor value).
5. **Calculate RD:** The drain voltage (VD) is typically aimed for VDD/2 to allow for maximum symmetrical output signal swing. VD=VDD−IDRD RD=IDVDD−VD (Use a standard resistor value).
6. **Calculate VDS:** VS=IDRS VDS=VD−VS=(VDD−IDRD)−(IDRS)=VDD−ID(RD+RS)
7. **Choose RG:** A large value like 1MΩ is typical, just to provide a DC path to ground for the gate and prevent static charge buildup.

6.1.5. Graphical Approach (Alternative for Design):

1. Plot the JFET's transfer characteristic (ID vs. VGS) using Shockley's Equation, for multiple points between VGS=0 (ID=IDSS) and VGS=VP (ID=0).
2. On the same graph, plot the self-bias line defined by VGS=−IDRS. This line passes through the origin (0,0). To plot it, pick a convenient ID (e.g., IDSS) and calculate the corresponding VGS=−IDSSRS. Plot this point and the origin, then draw a straight line.
3. The intersection of the transfer characteristic curve and the self-bias line gives the Q-point (ID,VGS). By adjusting RS, you can move this line and thus change the Q-point. Design involves iterating on RS until the intersection is at your desired ID and VGS.

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7. Pre-Lab Design and Calculations

7.1. BJT Voltage Divider Bias Design

Given Parameters:

- Transistor: NPN BJT (e.g., BC547)
- Supply Voltage: VCC=12V
- Target Q-point: IC=2mA, VCE=6V
- Assume minimum βDC for BC547 = 100 (refer to datasheet if available, otherwise use this value).
- Assume VBE=0.7V

Design Steps:

1. **Target IC=2mA, VCE=6V.**
2. **Calculate VE and RE:**
    - Let's aim for VE≈15% of VCC. VE=0.15×12V=1.8V.
    - RE=IEVE≈ICVE=2mA1.8V=900Ω.
    - **Choose Standard Resistor Value for RE:** [Write down chosen standard value, e.g., 820Ω or 1kΩ].
        - *Let's proceed with RE=820Ω for our calculation.*
        - *Recalculate VE with chosen RE: VE=IC×RE=2mA×820Ω=1.64V.* (This is the refined VE based on standard component availability).
3. **Calculate VC and RC:**
    - VC=VCE+VE=6V+1.64V=7.64V.
    - RC=ICVCC−VC=2mA12V−7.64V=2mA4.36V=2.18kΩ.
    - **Choose Standard Resistor Value for RC:** [Write down chosen standard value, e.g., 2.2kΩ].
        - *Let's proceed with RC=2.2kΩ.*
4. **Calculate VB:**
    - VB=VE+VBE=1.64V+0.7V=2.34V.
5. **Calculate R1 and R2 (Voltage Divider):**
    - Calculate IB: IB=βminIC=1002mA=20μA.
    - Choose IR2=10×IB=10×20μA=200μA.
    - R2=IR2VB=200μA2.34V=11.7kΩ.
    - **Choose Standard Resistor Value for R2:** [Write down chosen standard value, e.g., 12kΩ].
        - *Let's proceed with R2=12kΩ.*
    - R1=IR2+IBVCC−VB=200μA+20μA12V−2.34V=220μA9.66V=43.9kΩ.
    - **Choose Standard Resistor Value for R1:** [Write down chosen standard value, e.g., 43kΩ or 47kΩ].
        - *Let's proceed with R1=43kΩ.*

Summary of Designed Resistor Values (for BJT Voltage Divider Bias):

- R1=[ChosenR1 Value]
- R2=[ChosenR2 Value]
- RC=[ChosenRC Value]
- RE=[ChosenRE Value]

Theoretical Q-point (using chosen standard values and Exact Analysis for precision):

- Using R1=43kΩ, R2=12kΩ, RC=2.2kΩ, RE=820Ω, βDC=100, VBE=0.7V, VCC=12V.
- RTH=R1+R2R1R2=43k+12k43k×12k=55516kΩ≈9.38kΩ.
- VTH=VCC×R1+R2R2=12V×55k12k≈2.618V.
- IB=RTH+(βDC+1)REVTH−VBE=9.38kΩ+(101×820Ω)2.618V−0.7V=9.38kΩ+83.22kΩ 1.918V=92.6kΩ1.918V≈20.71μA.
- IC=βDCIB=100×20.71μA=2.071mA.
- IE=IC/α≈IC=2.071mA. (More precisely IE=(βDC+1)IB=101×20.71μA=2.09171mA)
- VE=IERE=2.09171mA×820Ω≈1.715V.
- VC=VCC−ICRC=12V−(2.071mA×2.2kΩ)=12V−4.5562V=7.4438V.
- VCE=VC−VE=7.4438V−1.715V=5.7288V.

Calculated Theoretical Q-point for Voltage Divider Bias:

- IC=[2.071mA]
- VCE=[5.7288V]

7.2. BJT Fixed Bias Design

Given Parameters:

- Transistor: NPN BJT (e.g., BC547)
- Supply Voltage: VCC=12V
- Target IC=2mA (to compare with voltage divider bias)
- Assume βDC=100
- Assume VBE=0.7V
- Aim for VCE=6V

Design Steps:

1. **Calculate IB:**
    - IB=βDCIC=1002mA=20μA.
2. **Calculate RB:**
    - RB=IBVCC−VBE=20μA12V−0.7V=20μA11.3V=565kΩ.
    - **Choose Standard Resistor Value for RB:** [Write down chosen standard value, e.g., 560kΩ].
        - *Let's proceed with RB=560kΩ.*
3. **Calculate RC:**
    - RC=ICVCC−VCE=2mA12V−6V=2mA6V=3kΩ.
    - **Choose Standard Resistor Value for RC:** [Write down chosen standard value, e.g., 3kΩ (or a combination like 2.7kΩ + 330Ω to get close if 3kΩ is not readily available as a single E24 value)].
        - *Let's proceed with RC=3kΩ.*

Summary of Designed Resistor Values (for BJT Fixed Bias):

- RB=[ChosenRB Value]
- RC=[ChosenRC Value]

Theoretical Q-point for Fixed Bias (using chosen standard values):

- Using RB=560kΩ, RC=3kΩ, βDC=100, VBE=0.7V, VCC=12V.
- IB=RBVCC−VBE=560kΩ12V−0.7V=560kΩ11.3V≈20.18μA.
- IC=βDCIB=100×20.18μA=2.018mA.
- VCE=VCC−ICRC=12V−(2.018mA×3kΩ)=12V−6.054V=5.946V.

Calculated Theoretical Q-point for Fixed Bias:

- IC=[2.018mA]
- VCE=[5.946V]

7.3. JFET Self-Bias Design

Given Parameters:

- Transistor: N-channel JFET (e.g., J201)
- Supply Voltage: VDD=15V
- Assume J201 parameters: IDSS=2mA, VP=−1V.
- Target ID=1mA (typically IDSS/2 for good operation).

Design Steps:

1. **Target ID=1mA.**
2. **Calculate VGS using Shockley's Equation:**
   - VGS=VP(1−IDSSID )
   - VGS=−1V(1−2mA1mA )=−1V(1−0.5 )
   - VGS=−1V(1−0.707)=−1V(0.293)=−0.293V.
3. **Calculate RS:**
   - RS=−IDVGS=−1mA−0.293V=293Ω.
   - **Choose Standard Resistor Value for RS:** [Write down chosen standard value, e.g., 270Ω or 330Ω].
     - *Let's proceed with RS=270Ω.*
     - *Recalculate VGS with RS=270Ω to see the effective VGS for ID=1mA: VGS=−1mA×270Ω=−0.27V.*
     - *Recalculate ID with the refined VGS value to see the actual Q-point for the chosen RS:*
       - ID=IDSS(1−VPVGS)2=2mA(1−−1V−0.27V)2=2mA(1−0.27)2=2mA(0.73)2=2mA×0.5329≈1.066mA. (This is the refined ID based on standard component availability).
4. **Calculate RD:**
   - Aim for VD≈VDD/2=15V/2=7.5V.
   - RD=IDVDD−VD=1.066mA15V−7.5V=1.066mA7.5V≈7.03kΩ.
   - **Choose Standard Resistor Value for RD:** [Write down chosen standard value, e.g., 6.8kΩ].

        - *Let's proceed with RD=6.8kΩ.*
5. **Choose RG:**
    - RG=1MΩ (standard practice for JFET gate).

Summary of Designed Resistor Values (for JFET Self-Bias):

- RG=[ChosenRG Value]
- RD=[ChosenRD Value]
- RS=[ChosenRS Value]

Theoretical Q-point for JFET Self-Bias (using chosen standard values):

- Using RG=1MΩ, RD=6.8kΩ, RS=270Ω, IDSS=2mA, VP=−1V, VDD=15V.
- From ID=2mA(1−−1VVGS)2 and VGS=−ID×270Ω.
- Solving these two equations (analytically or iteratively): ID≈1.066mA and VGS≈−0.288V.
- VS=IDRS=1.066mA×270Ω≈0.288V.
- VD=VDD−IDRD=15V−(1.066mA×6.8kΩ)=15V−7.249V=7.751V.
- VDS=VD−VS=7.751V−0.288V=7.463V.

Calculated Theoretical Q-point for JFET Self-Bias:

- ID=[1.066mA]
- VDS=[7.463V]
- VGS=[−0.288V]

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8. Circuit Diagrams

(Draw these clearly in your practical file. Use standard component symbols.)

8.1. BJT Voltage Divider Bias Circuit

[**Drawing Space:** A clear, labeled diagram of the NPN BJT Voltage Divider Bias circuit with VCC, R1, R2, RC, RE, and the NPN transistor (Emitter, Base, Collector labeled). Show ground connections.]

8.2. BJT Fixed Bias Circuit

[**Drawing Space:** A clear, labeled diagram of the NPN BJT Fixed Bias circuit with VCC, RB, RC, and the NPN transistor. Show ground connections.]

8.3. JFET Self-Bias Circuit

[**Drawing Space:** A clear, labeled diagram of the N-channel JFET Self-Bias circuit with VDD, RG, RD, RS, and the N-channel JFET (Gate, Drain, Source labeled). Show ground connections.]

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9. Procedure

9.1. BJT Voltage Divider Bias Implementation and Measurement

1. **Collect Components:** Gather all resistors ($R1, R2, RC, RE$) and the NPN BJT designed in Section 7.1.
2. **Construct Circuit:** Carefully assemble the BJT Voltage Divider Bias circuit on the breadboard as per your circuit diagram. Double-check all connections.
3. **Power On:** Connect the DC power supply to VCC (12V) and ground. **Ensure the power supply is OFF before connecting.**
4. **Initial Check:** Before powering ON, perform a quick visual inspection for any short circuits or incorrect connections.
5. **Apply Power:** Turn on the DC power supply.
6. **Measure Q-point:** Using the Digital Multimeter (DMM) in DC voltage mode, measure the following voltages with respect to ground:
    - VC (Collector Voltage)
    - VB (Base Voltage)
    - VE (Emitter Voltage)
    - Record these values in Table 9.1.1.
7. **Calculate VCE and IC:**
    - $VCE = VC - VE$
    - $IC \approx IE = VE/RE$ (Use the actual measured VE and the nominal value of RE).
    - Record these calculated values in Table 9.1.1.
8. **Compare:** Compare the measured Q-point (IC,VCE) with your theoretically calculated Q-point from Section 7.1. Note any differences.
9. **Power Off:** Turn off the DC power supply.

9.2. BJT Fixed Bias Implementation and Stability Comparison

1. **Collect Components:** Gather all resistors (RB, RC) and a new NPN BJT (of the same type as used in 9.1) designed in Section 7.2.
2. **Construct Circuit:** Carefully assemble the BJT Fixed Bias circuit on the breadboard.
3. **Power On:** Connect the DC power supply to VCC (12V) and ground. Ensure power supply is OFF before connecting.
4. **Initial Check:** Visual inspection.
5. **Apply Power:** Turn on the DC power supply.
6. **Measure Q-point (Fixed Bias - Initial):**
    - Measure VCE (Collector-Emitter Voltage).
    - Measure VC (Collector Voltage).
    - Record these values in Table 9.2.1.
7. **Calculate IC (Fixed Bias - Initial):**
    - $IC = (VCC - VC)/RC$ (Use the actual measured VC and nominal RC).
    - Record this calculated value in Table 9.2.1.
8. **Stability Test - Temperature Variation (Fixed Bias):**
    - While the circuit is powered on, gently warm the transistor (e.g., by holding it between your fingers or using warm air from a safe distance for a very brief period).

    - Observe and note the immediate change in VCE and calculate IC. **Do not overheat the transistor.**
    - Record these observed values in Table 9.2.1. Let the transistor cool down and return to its initial state.
9. **Stability Test - Transistor Replacement (Fixed Bias):**
    - **Power OFF.** Carefully replace the current NPN BJT with a *different* NPN BJT of the same type (e.g., another BC547).
    - **Power ON.** Measure and record the new VCE and calculate IC.
    - Record these values in Table 9.2.1.
10. **Power Off:** Turn off the DC power supply and carefully remove the Fixed Bias circuit components.
11. **Stability Test - Temperature Variation (Voltage Divider Bias):**
    - Reconstruct or retrieve your Voltage Divider Bias circuit from Section 9.1.
    - **Power ON.** Measure and note the initial VCE and IC.
    - Gently warm the transistor as before. Observe and note the change in VCE and IC.
    - Record these values in Table 9.2.2.
12. **Stability Test - Transistor Replacement (Voltage Divider Bias):**
    - **Power OFF.** Replace the NPN BJT with a *different* NPN BJT of the same type.
    - **Power ON.** Measure and record the new VCE and IC.
    - Record these values in Table 9.2.2.
13. **Power Off:** Turn off the DC power supply.

9.3. JFET Self-Bias Implementation and Measurement

1. **Collect Components:** Gather all resistors (RG,RD,RS) and the N-channel JFET designed in Section 7.3.
2. **Construct Circuit:** Carefully assemble the JFET Self-Bias circuit on the breadboard. Ensure RG is connected between the Gate and Ground.
3. **Power On:** Connect the DC power supply to VDD (15V) and ground. **Ensure the power supply is OFF before connecting.**
4. **Initial Check:** Visual inspection.
5. **Apply Power:** Turn on the DC power supply.
6. **Measure Q-point:** Using the DMM, measure the following voltages with respect to ground:
    - VD (Drain Voltage)
    - VS (Source Voltage)
    - VG (Gate Voltage - should be close to 0V).
    - Record these values in Table 9.3.1.
7. **Calculate ID, VGS, and VDS:**
    - ID=VS/RS (Use the actual measured VS and nominal RS).
    - VGS=VG−VS (Note: VG should be ~0V).
    - VDS=VD−VS
    - Record these calculated values in Table 9.3.1.
8. **Compare:** Compare the measured Q-point (ID,VDS,VGS) with your theoretically calculated Q-point from Section 7.3.

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10. Observations and Readings

10.1. BJT Voltage Divider Bias Readings

Designed Component Values:

- $R_1 = $ [Value]
- $R_2 = $ [Value]
- $R_C = $ [Value]
- $R_E = $ [Value]

Table 10.1.1: BJT Voltage Divider Bias Q-point Measurement

Parameter	Theoretical Value	Measured Value	Calculated from Measured
VB	[from 7.1]		N/A
VE	[from 7.1]		N/A
VC	[from 7.1]		N/A
IC	[from 7.1]	N/A	IC=VE/RE
VCE	[from 7.1]	N/A	VCE=VC−VE

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10.2. BJT Fixed Bias vs. Voltage Divider Bias Stability Readings

Designed Component Values (Fixed Bias):

- $R_B = $ [Value]
- $R_C = $ [Value]

Table 10.2.1: BJT Fixed Bias Stability Observations

Condition	Measured VCE	Calculated IC=(VCC−VC)/RC (where VC is measured)	Observations / Remarks (Q-point Shift)
Initial (after construction)			
Transistor Warmed			
Transistor Replaced (2nd BJT)			

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Table 10.2.2: BJT Voltage Divider Bias Stability Observations

Condition	Measured VCE	Calculated IC=VE/RE (where VE is measured)	Observations / Remarks (Q-point Shift)
Initial (after construction)			
Transistor Warmed			
Transistor Replaced (2nd BJT)			

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10.3. JFET Self-Bias Readings

Designed Component Values:

- $R_G = $ [Value]
- $R_D = $ [Value]
- $R_S = $ [Value]

Table 10.3.1: JFET Self-Bias Q-point Measurement

Parameter	Theoretical Value	Measured Value	Calculated from Measured
VD	[from 7.3]		N/A
VS	[from 7.3]		N/A
VG	[from 7.3]		N/A
ID	[from 7.3]	N/A	ID=VS/RS
VGS	[from 7.3]	N/A	VGS=VG−VS
VDS	[from 7.3]	N/A	VDS=VD−VS

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11. Calculations

(Show all detailed calculations here, ideally replicating your pre-lab calculations using your chosen standard component values, and then using your *measured* values to calculate the actual Q-points for comparison.)

11.1. BJT Voltage Divider Bias Calculations:

- Show calculation of theoretical Q-point with chosen standard resistors.
- Show calculation of IC and VCE using your measured VE, VC, and RE from Table 10.1.1.

11.2. BJT Fixed Bias Calculations:

- Show calculation of theoretical Q-point with chosen standard resistors.
- Show calculations of IC and VCE for all three conditions (initial, warmed, replaced) from Table 10.2.1, using your measured VC and VCE and nominal RC.

11.3. JFET Self-Bias Calculations:

- Show calculation of theoretical Q-point with chosen standard resistors.
- Show calculation of ID, VGS, and VDS using your measured VG, VD, VS, RS, and RD from Table 10.3.1.

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12. Results and Discussion

(Analyze your observations and calculations thoroughly here.)

12.1. BJT Voltage Divider Bias:

- Compare your measured Q-point with your theoretical Q-point. Discuss any discrepancies. Are they within acceptable tolerance (e.g., due to resistor tolerance, actual β of the transistor vs. assumed β)?
- State the final measured Q-point for the voltage divider bias circuit.

12.2. BJT Fixed Bias vs. Voltage Divider Bias Stability:

- **Fixed Bias Analysis:** Describe the observed changes in VCE and IC when the transistor was warmed and when it was replaced. Quantify the percentage change in IC for each case if possible. Explain *why* these changes occurred (referencing β dependence).
- **Voltage Divider Bias Analysis:** Describe the observed changes in VCE and IC for the voltage divider bias circuit under the same conditions (warmed, replaced). Quantify the percentage change.
- **Comparison:** Explicitly compare the degree of Q-point shift between the fixed bias and voltage divider bias circuits. Which circuit demonstrated better stability? Explain in detail *why* the voltage divider bias is more stable, referencing the role of the emitter resistor RE and the base voltage divider.

12.3. JFET Self-Bias:

- Compare your measured Q-point (ID,VDS,VGS) with your theoretical Q-point. Discuss any discrepancies (e.g., due to variations in actual IDSS and VP of the JFET).
- State the final measured Q-point for the JFET self-bias circuit.
- Explain the role of RS in providing self-bias and stability for the JFET circuit.

12.4. Advantages and Disadvantages of Biasing Schemes:

Based on your design experience and experimental observations, discuss the merits and demerits of each biasing scheme:

- **BJT Fixed Bias:**
  - **Advantages:** [List]
  - **Disadvantages:** [List] (Emphasize lack of stability).
- **BJT Voltage Divider Bias:**
  - **Advantages:** [List] (Emphasize stability, common use).
  - **Disadvantages:** [List] (e.g., more components).
- **JFET Self-Bias:**
  - **Advantages:** [List] (Emphasize simplicity, good stability for JFETs, single supply).
  - **Disadvantages:** [List] (e.g., Q-point calculation can be more complex due to non-linearity, parameter variations can still be an issue if not accounted for).

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13. Conclusion

Summarize the key findings of the experiment. Reiterate the importance of proper biasing for stable amplifier operation. Conclude on which biasing scheme is generally preferred for BJTs and JFETs based on stability and practicality, linking back to your experimental results.

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14. Viva-Voce Questions (For Instructor/Self-Study)

1. What is the purpose of biasing a transistor?
2. What is a Q-point and why is it important to keep it stable?
3. Why is Fixed Bias considered unstable for BJTs?
4. How does the emitter resistor (RE) in a BJT voltage divider bias circuit contribute to stability?
5. What is the significance of the 10IB rule in voltage divider bias design?
6. How does an N-channel JFET's VGS become negative in a self-bias configuration?
7. What is Shockley's Equation and how is it used in JFET biasing?
8. What happens to the Q-point if a BJT's βDC increases significantly? Which biasing method is more affected?
9. List two factors that can cause a transistor's parameters to vary.
10. If the Q-point shifts too close to the cutoff region, what will be the effect on the amplifier's output signal?